SPECIFICATIONS

Product Type  1/3-type Progressive Scan Color CCD Area Sensor with 350k Pixels (1ch)

Model No  R J 3 3 B 3 A A 0 D T

※ This specifications contains 20 pages including the cover and appendix.
   If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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BY :

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PREPARED BY :  T. Kenzaki

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SHARP CORPORATION
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(2) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (3), even for the following application areas, be sure to observe the precautions given in Paragraph (3). Never use the products for the equipment listed in Paragraph (4).

Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliance
- Communication equipment other than for trunk lines

(3) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc

(4) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(5) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

○ Please direct all queries and regarding the products covered herein to a sales representative of the company.
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The RJ33B3AA0DT is a 1/3-type solid-state image sensor that consists of PN photo-diodes and CCDs (charge-coupled devices, 1ch). With approximately 359k pixels, the sensor provides a high resolution stable color image.

1.1 Features

1) Optical size: 5.92 mm (Aspect ratio 4:3)
2) Progressive scan format
3) Square pixel
4) Number of total pixels: Horizontal 716 × Vertical 502
   Number of image pixels: Horizontal 660 × Vertical 494
   Number of effective pixels: Horizontal 640 × Vertical 480
   Pixel pitch: Horizontal 7.4 μm × Vertical 7.4 μm
   Number of optical black pixels: Horizontal: 28 front 28 rear
                                Vertical: 6 front 2 rear
   Number of dummy bits: Horizontal: 4 front, Vertical: 2 front
5) R, G and B primary color mosaic filters
6) Built-in overflow drain voltage output circuit, and reset gate voltage circuit
7) Variable electronic shutter
8) Low fixed pattern noise and lag
9) No burn-in and no image distortion
10) Blooming suppression structure
11) Built-in output amplifier
12) N-type silicon substrate, N-MOS process,
    Not designed or rated as radiation hardened
13) Global shutter

1.2 Applications

1) Industrial monitor cameras
2) Video capturing devices for PCs, etc.

"iSHCCD II", "iSHCCD" and "iSHartina" are the trademarks of Sharp Corporation. The "iSHCCD II" is an advanced CCD image sensor that drastically improves light efficiency by including near-infrared light region as a basic structure of "iSHCCD". The "iSHartina" series is a key device group of Sharp which realizes a next-generation sensing world.

The circuit diagram and others included in this specifications are intended for use to explain typical application examples. Therefore, we take no responsibility for any problem as may occur due to the use of the included circuit and for any problem with industrial proprietary rights or other rights.
2 ARRANGEMENT OF PIXELS AND COLOR FILTERS

Optical black (28 pixels)

Image pixels
660(H) × 494(V)

Optical black (28 pixels)

Optical black (6 pixels)

Dummy bit (2 pixels)

(1, 494) (660, 494)

G B G B G B G B G B G B G B G B G B G
R G R G R G R G R G R G R G R G R G R G
G B G B G B G B G B G B G B G B G B G
R G R G R G R G R G R G R G R G R G R G
G B G B G B G B G B G B G B G B G B G
R G R G R G R G R G R G R G R G R G R G

(1, 1) (660, 1)
3 PIN CONFIGURATION (TOP VIEW)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODa</td>
<td>Output transistor drain</td>
</tr>
<tr>
<td>OSa</td>
<td>Output signals</td>
</tr>
<tr>
<td>φ RSa</td>
<td>Reset transistor clock</td>
</tr>
<tr>
<td>φ V1, φV2, φV3, φV4</td>
<td>Vertical shift register clock</td>
</tr>
<tr>
<td>φ LH1a, φH1a, φH2a, φH1b, φH2b</td>
<td>Horizontal shift register clock</td>
</tr>
<tr>
<td>OFD</td>
<td>Overflow drain</td>
</tr>
<tr>
<td>OOFD</td>
<td>Output overflow drain</td>
</tr>
<tr>
<td>PW</td>
<td>P_well</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>RSCT</td>
<td>Reset control</td>
</tr>
</tbody>
</table>

4 ABSOLUTE MAXIMUM RATINGS \((T_A=25°C)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output transistor drain voltage</td>
<td>VOD</td>
<td>0 to +15.4</td>
<td>V</td>
</tr>
<tr>
<td>Overflow drain voltage</td>
<td>VOFD</td>
<td>0 to +32</td>
<td>V</td>
</tr>
<tr>
<td>Overflow drain output voltage</td>
<td>V0OFD</td>
<td>Internal output (Note 1)</td>
<td></td>
</tr>
<tr>
<td>Reset gate clock voltage</td>
<td>V φ RS</td>
<td>Internal output (Note 2)</td>
<td></td>
</tr>
<tr>
<td>Vertical shift register clock voltage</td>
<td>V φ V</td>
<td>VPW to +15.4</td>
<td>V</td>
</tr>
<tr>
<td>Horizontal shift register clock voltage</td>
<td>V φ H</td>
<td>-0.3 to +7</td>
<td>V</td>
</tr>
<tr>
<td>Voltage difference between P_well and vertical clock</td>
<td>V PW-V φ V</td>
<td>-23.8 to +0</td>
<td>V</td>
</tr>
<tr>
<td>Voltage difference between vertical clocks</td>
<td>V φ V-V φ V</td>
<td>0 to +9.9 (Note 3)</td>
<td>V</td>
</tr>
<tr>
<td>Reset control voltage</td>
<td>VRSCT</td>
<td>-0.3 to +7</td>
<td>V</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>TSTG</td>
<td>-40 to +90</td>
<td>°C</td>
</tr>
<tr>
<td>Ambient operating temperature</td>
<td>TTOPR</td>
<td>-30 to +85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(Note 1) Use the circuit parameter indicated in “8. EXAMPLE OF STANDARD OPERATING CIRCUIT” and do not connect to DC voltage directly. When OOFD is connected to GND, connect VOD to GND.

(Note 2) Do not connect to DC voltage directly. When φ RS is connected to GND, connect VOD to GND. Reset gate clock is applied below 5.1 Vp-p.

(Note 3) When clock width is below 10 μs, and clock duty factor is below 0.1 %, voltage difference between adjoining vertical clocks are guaranteed up to 15.4 V.

Do not change all φ V during 0.5 μs before rising edge of V φ VH pulse and after falling edge of V φ VH pulse.

Do not change directly into V φ VL → V φ VH or V φ VH → V φ VL.
5 RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient operating temperature</td>
<td>$T_{\text{OPR}}$</td>
<td>25.0</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Output transistor drain voltage</td>
<td>$V_{\text{ODa}}$</td>
<td>13.1</td>
<td>13.5</td>
<td>13.9</td>
<td>V</td>
</tr>
<tr>
<td>Overflow drain clock p-p level</td>
<td>$V_{\phi\text{OFD}}$</td>
<td>19.3</td>
<td>20.0</td>
<td>20.7</td>
<td>V</td>
</tr>
<tr>
<td>Ground</td>
<td>GND</td>
<td>0.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>P_well voltage</td>
<td>$V_{\text{PW}}$</td>
<td>-6.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Vertical shift register clock</td>
<td>$V_{\phi\text{VIL}}, V_{\phi\text{VIL}}, V_{\phi\text{VIL}}, V_{\phi\text{VIL}}$</td>
<td>-6.8</td>
<td>-6.5</td>
<td>-6.2</td>
<td>V</td>
</tr>
<tr>
<td>INTERMEDIATE level</td>
<td>$V_{\phi\text{VIL}}, V_{\phi\text{VIL}}, V_{\phi\text{VIL}}, V_{\phi\text{VIL}}$</td>
<td>0.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>HIGH level</td>
<td>$V_{\phi\text{VIL}}$</td>
<td>13.1</td>
<td>13.5</td>
<td>13.9</td>
<td>V</td>
</tr>
<tr>
<td>Horizontal shift register clock</td>
<td>$V_{\phi\text{HIL}}, V_{\phi\text{HIL}}, V_{\phi\text{HIL}}, V_{\phi\text{HIL}}$</td>
<td>-0.05</td>
<td>0.0</td>
<td>0.05</td>
<td>V</td>
</tr>
<tr>
<td>HIGH level</td>
<td>$V_{\phi\text{HIL}}, V_{\phi\text{HIL}}, V_{\phi\text{HIL}}, V_{\phi\text{HIL}}$</td>
<td>3.15</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Reset gate clock</td>
<td>$V_{\phi\text{RSa}}$</td>
<td>5.15</td>
<td>3.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Reset control voltage (Note 4)</td>
<td>$V_{\text{RCT}}$</td>
<td>2.8</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Vertical shift register clock frequency (Note 3)</td>
<td>$f_{\phi\text{V1}}, f_{\phi\text{V2}}, f_{\phi\text{V3}}, f_{\phi\text{V4}}$</td>
<td>60.7</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Horizontal shift register clock frequency</td>
<td>$f_{\phi\text{H1a}}, f_{\phi\text{H1b}}, f_{\phi\text{H2a}}, f_{\phi\text{H2b}}$</td>
<td>60.0</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset gate clock frequency</td>
<td>$f_{\phi\text{RSa}}$</td>
<td>60.0</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Nota 1) Use the circuit parameter indicated in “EXAMPLE OF STANDARD OPERATING CIRCUIT”, and do not connect to DC voltage directly.

(Note 2) $V_{\text{PW}}$ is set below $V_{\phi\text{VL}}$ that is low level of vertical shift register clock, or is used with the same power supply that is connected to $V_L$ of V driver IC.

(Note 3) At frame accumulation mode.

(Note 4) Do not use $V_{\text{RCT}}$ HIGH(2.8 to 3.6V) in case $V_{\phi\text{RSa}}$ is set as 3.15 to 4.5V.

Refer to the relationship of Reset gate clock voltage and Reset control voltage as following table.

<table>
<thead>
<tr>
<th>Reset gate clock voltage</th>
<th>Reset control voltage</th>
<th>Saturation output voltage</th>
<th>Min.</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.5 to 5.5 V</td>
<td>LOW(0V)</td>
<td>1000mV</td>
<td></td>
</tr>
<tr>
<td>3.15 to 4.5 V</td>
<td>HIGH(2.8 to 3.6V)</td>
<td>1500mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LOW(0V)</td>
<td>1000mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HIGH(2.8 to 3.6V)</td>
<td>Caution :prohibition</td>
<td></td>
</tr>
</tbody>
</table>

※ To apply power, first connect GND and then turn on $V_{\text{OD}}$. After turning on $V_{\text{OD}}$, turn on $V_{\text{PW}}$ first and then turn on other powers and pulses.

Do not connect the device to or disconnect it from the plug socket while power is being applied.
6 CHARACTERISTICS (Drive method : 1/30s frame accumulation)

$T_A : +25^\circ C$, but $+60^\circ C$ for parameter No.4 and No.5.

Operating conditions : the typical values specified in “5 RECOMMENDED OPERATING CONDITIONS”.

Color temperature of light source : 3200K, IR cut-off filter (CM-500,1 mm) is used.

<table>
<thead>
<tr>
<th>No.</th>
<th>Parameter</th>
<th>Symbol</th>
<th>Note</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Standard output voltage</td>
<td>$V_O$</td>
<td>1</td>
<td>150</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>2</td>
<td>Photo response non-uniformity</td>
<td>PRNU</td>
<td>2</td>
<td></td>
<td>10%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Saturation output voltage</td>
<td>$V_{SAT}$</td>
<td>3</td>
<td>1000※</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>4</td>
<td>Dark output voltage</td>
<td>$V_{DARK}$</td>
<td>4</td>
<td>0.5</td>
<td>3.0</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>5</td>
<td>Dark signal non-uniformity</td>
<td>DSNU</td>
<td>5</td>
<td>0.5</td>
<td>2.0</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>6</td>
<td>Sensitivity (Green channel)</td>
<td>$R(G)$</td>
<td>6</td>
<td>2400</td>
<td></td>
<td>3000</td>
<td>mV</td>
</tr>
<tr>
<td>7</td>
<td>Smear ratio</td>
<td>SMR</td>
<td>7</td>
<td>-125</td>
<td>-110</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>8</td>
<td>Image lag</td>
<td>AI</td>
<td>8</td>
<td></td>
<td>1.0</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>9</td>
<td>Blooming suppression ratio</td>
<td>ABL</td>
<td>9</td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Output transistor drain current</td>
<td>$I_{OD}$</td>
<td>6.0</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

【 Notes 】
1. The average output voltage of G signal under the uniform illumination. The standard exposure conditions are defined as when $V_O$ is 150 mV.
2. The image area is divided into 10 × 10 segments under the standard exposure conditions. Each segment’s voltage is the average output voltage of all pixels within the segment. PRNU is defined by $(V_{max} – V_{min}) / V_O$, where $V_{max}$ and $V_{min}$ are the maximum and minimum values of each segment’s voltage respectively.
3. The image area is divided into 10 × 10 segments. Each segment’s voltage is the average output voltages of all pixels within the segment. $V_{SAT}$ is the minimum segment’s voltage under 20 times exposure of the standard exposure conditions.
4. The average output voltage under non-exposure conditions.
5. The image area is divided into 10 × 10 segments under non-exposure conditions. DSNU is defined by $(V_{dmax} – V_{dmin})$, where $V_{dmax}$ and $V_{dmin}$ are the maximum and minimum values of each segment’s voltage respectively.
6. The average output voltage of G signal when a 1000 lux light source with a 90 % reflector is imaged by a lens of F4, f50 mm.
7. The sensor is exposed only in the central area of V/10 square with a lens at F4, where V is the vertical image size. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum output voltage in the V/10 square.
8. The sensor is exposed at the exposure level corresponding to the standard conditions. AI is defined by the ratio of the output voltage measured at the 1st field during the non-exposure period to the standard output voltage.
9. The sensor is exposed only in the central area of V/10 square, where V is the vertical image size. ABL is defined by the ratio of the exposure at the standard conditions to the exposure at a point where blooming is observed.
※ $V_{SAT}$ depend on the applied voltage of $V_{RSC}$ and $V_{\phi}$Ref. Refer to the relationship of $V_{RSC}$ and $V_{\phi}$Ref indicated in “5 RECOMMENDED OPERATING CONDITIONS” (Note4).

【 Comment 】
Within the recommended operating conditions of $V_{OD}$, $V_{OD}$ of the internal output satisfies with ABL and $V_{SAT}$.
Vertical transfer timing【All-pixel readout mode】fck=60MHz 120fps

Pulse diagram in move detail is shown in figures (ⅰ) to (ⅱ) after next page

<table>
<thead>
<tr>
<th>HD No.</th>
<th>HD</th>
<th>VD</th>
<th>φ V1</th>
<th>φ V2</th>
<th>φ V3</th>
<th>φ V4</th>
<th>φ OFD</th>
<th>O Sa</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Readout timing [All-pixel readout mode] \( f_{ck}=60\text{MHz} \) 120fps (i)

- \( \phi \text{H1a, H1b} \)
- \( \phi \text{H2a, H2b} \)
- \( \phi \text{RSa} \)
- \( \phi \text{OSa} \)
- \( \phi \text{V1} \)
- \( \phi \text{V2} \)
- \( \phi \text{V3} \)
- \( \phi \text{V4} \)
- \( \phi \text{OFD} \)

* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.
* Keep over the periods indicated in this timing chart when vertical transfer clock pulse is overlapping.
EXAMPLE OF STANDARD OPERATING CIRCUIT

- 10 μF 2SC1623/2SC4617 or equivalent
- 47 Ω 1S2837/DA121 or equivalent 100k Ω or equivalent
- VH 100k Ω 680pF
- 0.1 μF R ≦ 2.2 Ω
- VDD + VH VL

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9 SPECIFICATION FOR BLEMISH (1/30 s frame accumulation)

1) Definition of blemish

<table>
<thead>
<tr>
<th></th>
<th>Level of blemish (mV)</th>
<th>Permitted number of blemish</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>White blemish</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Exposed)</td>
<td>100 ≤ B</td>
<td>0</td>
<td>• See fig.9-1(a), fig.9-2.</td>
</tr>
<tr>
<td></td>
<td>B &lt; 100</td>
<td>no count</td>
<td>• Vout = Vstd</td>
</tr>
<tr>
<td>Black blemish</td>
<td>120 ≤ B</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>(Exposed)</td>
<td>55 ≤ B &lt; 120</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>40 ≤ B &lt; 55</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B &lt; 40</td>
<td>no count</td>
<td></td>
</tr>
<tr>
<td>White blemish</td>
<td>100 &lt; B</td>
<td>0</td>
<td>• See fig.9-1(b), fig.9-2</td>
</tr>
<tr>
<td>(Non-Exposed)</td>
<td>20 &lt; B ≤ 100</td>
<td>N</td>
<td>• N ≤ 10</td>
</tr>
<tr>
<td></td>
<td>2.5 &lt; B ≤ 20</td>
<td>M</td>
<td>• M + N ≤ 50</td>
</tr>
<tr>
<td></td>
<td>B &lt; 2.5</td>
<td>no count</td>
<td></td>
</tr>
<tr>
<td>White blemish</td>
<td>5.0 ≤ B</td>
<td>0</td>
<td>• See fig.9-1(a), fig.9-2</td>
</tr>
<tr>
<td>(Shutter mode)</td>
<td>B &lt; 5.0</td>
<td>no count</td>
<td>• Vout = Vstd/10</td>
</tr>
<tr>
<td>Black blemish</td>
<td>5.0 ≤ B</td>
<td>0</td>
<td>• The electronic shutter speed is set at 1/10000 s</td>
</tr>
<tr>
<td>(Shutter mode)</td>
<td>B &lt; 5.0</td>
<td>no count</td>
<td></td>
</tr>
</tbody>
</table>

- B : Blemish level defined in fig. 9-1.
- Vout : Average output voltage
- Vstd : 150 mV (The average output voltage of G signal). The standard output voltage defined in the specification of the characteristics.
【MEASURING CONDITION】

- Ta: 60 °C
- Measuring block diagram

The output voltage is measured at the CCD output.
The gain of the amplifier is adjusted to the unity between the CCD output and the amplifier output.

【MEASURING AREA】

fig. 9-2 Definition of the measuring area
(The wave form is the luminance signal measured at the Amplifier output)
PRECAUTIONS

10.1 Package Breakage

In order to prevent the package from being broken, observe the following instructions:

1) The CCD is a precise optical component and the package material is plastic. Therefore,
   • Take care not to drop the device when mounting, handling, or transporting.
   • Avoid giving a shock to the package. Especially when leads are fixed to the socket or the circuit board, small shock could break the package more easily than when the package isn’t fixed.

2) When mounting the package on the housing, be sure that the package is not bent.
   — If a bent package is forced into place between a hard plate or the like, the package may be broken.

3) If any damage or breakage occurs on the surface of the glass cap, its characteristics could deteriorate. Therefore,
   • Do not hit the glass cap.
   • Do not give a shock large enough to cause distortion.
   • Do not scrub or scratch the glass surface.
   — Even a soft cloth or applicator, if dry, could cause flaws to scratch the glass.

10.2 Electrostatic Damage

As compared with general MOS-LSI, CCD has lower ESD. Therefore, take the following antistatic measures when handling the CCD:

1) Always discharge static electricity by grounding the human body and the instrument to be used. To ground the human body, provide resistance of about 1 MΩ between the human body and the ground to be on the safe side.

2) When directly handling the device with the fingers, hold the part without leads and do not touch any lead.

3) To avoid generating static electricity,
   a. do not scrub the glass surface with cloth or plastic
   b. do not attach any tape or labels
   c. do not clean the glass surface with dust-cleaning tape

4) When storing or transporting the device, put it in a container of conductive material.
10.3 Dust and Contamination

Dust or contamination on the glass surface could deteriorate the output characteristics or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

1) Handle the CCD in a clean environment such as a cleaned booth. (The cleanliness level should be, if possible, class 1,000 at least.)

2) Do not touch the glass surface with the fingers. If dust or contamination gets on the glass surface, the following cleaning method is recommended:
   - Dust from static electricity should be blown off with an ionized air blower. For anti-electrostatic measures, however, ground all the leads on the device before blowing off the dust.
   - The contamination on the glass surface should be wiped off with a clean applicator soaked in Isopropyl alcohol. Wipe slowly and gently in one direction only.
   - Frequently replace the applicator and do not use the same applicator to clean more than one device.

※ Note: In most cases, dust and contamination are unavoidable, even before the device is first used. It is, therefore, recommend that the above procedures should be taken to wipe out dust and contamination before using the device.

10.4 Other

1) Soldering should be manually performed within 5 seconds at 350°C maximum at the tip of soldering iron.

2) Avoid using or storing the CCD at high temperature or high humidity as it is a precise optical component. Do not give a mechanical shock to the CCD.

3) CCD has the possibility that white blemish, which originates in the structure of CCD with the passage of time by an external factor such as the radiations, could be generated. Please use white blemish compensation circuit for white blemish generated afterward.

4) Do not expose the device to strong light. For the color device, long exposure to strong light will fade the color of the color filters.
11 PACKAGE OUTLINE AND PACKING SPECIFICATION

11 1. Package Outline Specification
   Refer to attached drawing.
   (The seal resin stick out from the package shall be passed. And, the seal resins are two kinds of colors, while and transparency.)

11 2. Markings
   Marking contents
   (1) Product name : RJ33B3AA0DT
   (2) Company name : SHARP
   (3) Country of origin : JAPAN
   (4) Date code : YY WW X XX
      Denotes the production ref. code.(2 figures)
      Denotes the production day of the week.
      Denotes the production week.
      (01,02,03,..,52,53)
      Denotes the production year.
      (Lower two digits of the year.)

   Positions of markings are shown in the package outline drawing.
   But, markings shown in that drawing are not provided any measurements of their characters and their positions.

11 3. Packing Specification
   3-1. Packing materials
      | Material Name | Material Spec. | Purpose                      |
      |---------------|----------------|-----------------------------|
      | Cover Tape    | Plastic film(1device/tape) | Glass lid covering         |
      | Device case   | Cardboard(540devices/case)  | Device tray fixing         |
      | Device tray   | Conductive plastic (90devices/tray) | Device packing(6trays/case) |
      | Cover tray    | Conductive plastic(1tray/case) | Device packing             |
      | PP band       | Polypropylene             | Device tray fixing         |
      | Buffer        | Cardboard(2sheets/case)   | Shock absorber of device tray |
      | Plastic film bag | Plastic film   | Device tray fixing         |
      | Tape          | Paper                     | Sealing plastic film bag and device case |
      | Label         | Paper                     | Indicates part number, quantity and date of manufacture |

   3-2. External appearance of packing
      Refer to attached drawing

11 4. Precaution
   1) Before unpacking, confirm the imports of the chapter "Handling Precaution" in this device specification.
   2) Unpacking should be done on the stand treated with anti-ESD. At that time, the same anti-ESD treatment should be done to operator's body, too.
5. Chemical substance information in the product

Product Information Notification based on Chinese law, Management Methods for Controlling Pollution by Electronic Information Products.

Names and Contents of the Hazardous Substances.

<table>
<thead>
<tr>
<th>Hazardous Substances</th>
<th>Lead (Pb)</th>
<th>Mercury (Hg)</th>
<th>Cadmium (Cd)</th>
<th>Hexavalent Chromium (Cr(VI))</th>
<th>Polybrominated Biphenyls (PBB)</th>
<th>Polybrominated Diphenyl Ethers (PBDE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
<td>○</td>
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<td>○</td>
</tr>
</tbody>
</table>

This table is prepared in accordance with the provisions of SJ/T 11364.

○ : Indicates that said hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement of GB/T 26572.

× : Indicates that said hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement of GB/T 26572.